Refine Search

Search Results -

Terms	Documents
((bus-repeater) or (bus adj1 repeater)) and lock$3	84

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, August 24, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L2	((bus-repeater) or (bus adj1 repeater)) and lock$3	84	L2
L1	((bus-repeater) or (bus adj1 repeater)) same lock$3	5	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L2	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, August 24, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=USPT,USOC; PLUR=YES; OP=OR			
L2	((bus-repeater) or (bus adj1 repeater)) and lock$3	84	L2
L1	((bus-repeater) or (bus adj1 repeater)) same lock$3	5	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(375/211 |709/239 |709/253 |370/351 |370/287 |370/492 |370/501 |710/305 |710/31 |710/306 |710/313 |710/314 |710/105 |710/200 |340/825.5 |326/104).ccls.	5500

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, August 24, 2004 Printable Copy Create Case

Set Name side by side	Query
	DB=USPT,USOC; PLUR=YES; OP=OR
L4	710/305,31,306,313,314,105,200;370/351,287,492,501;709/239,253;375/211;326/104;340/825.5.
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L3	L2
	DB=USPT,USOC; PLUR=YES; OP=OR
L2	((bus-repeater) or (bus adj1 repeater)) and lock$3
L1	((bus-repeater) or (bus adj1 repeater)) same lock$3

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L2 and L4	8

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text | Clear | Interrupt

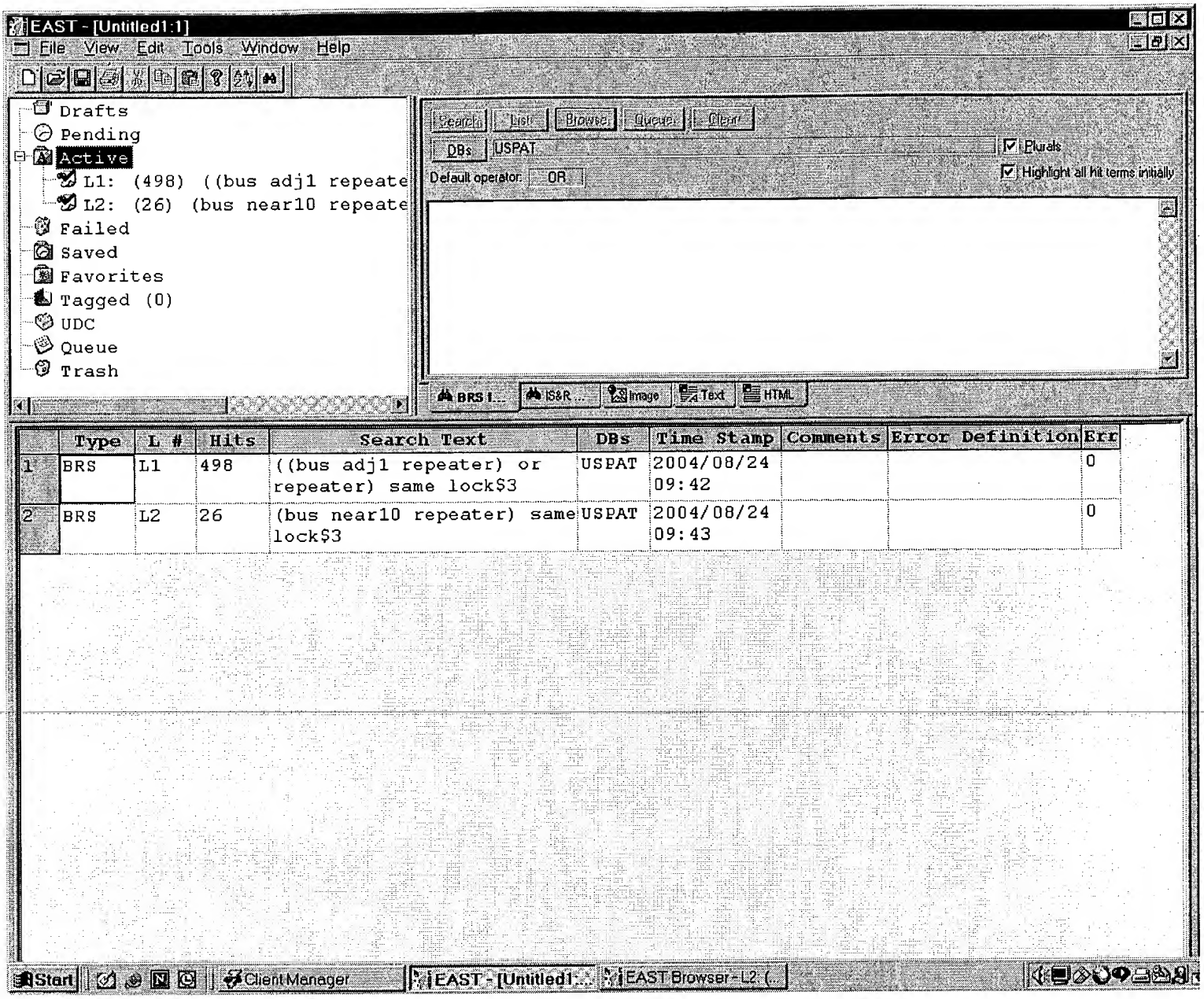
Search History

DATE: Tuesday, August 24, 2004 Printable Copy Create Case

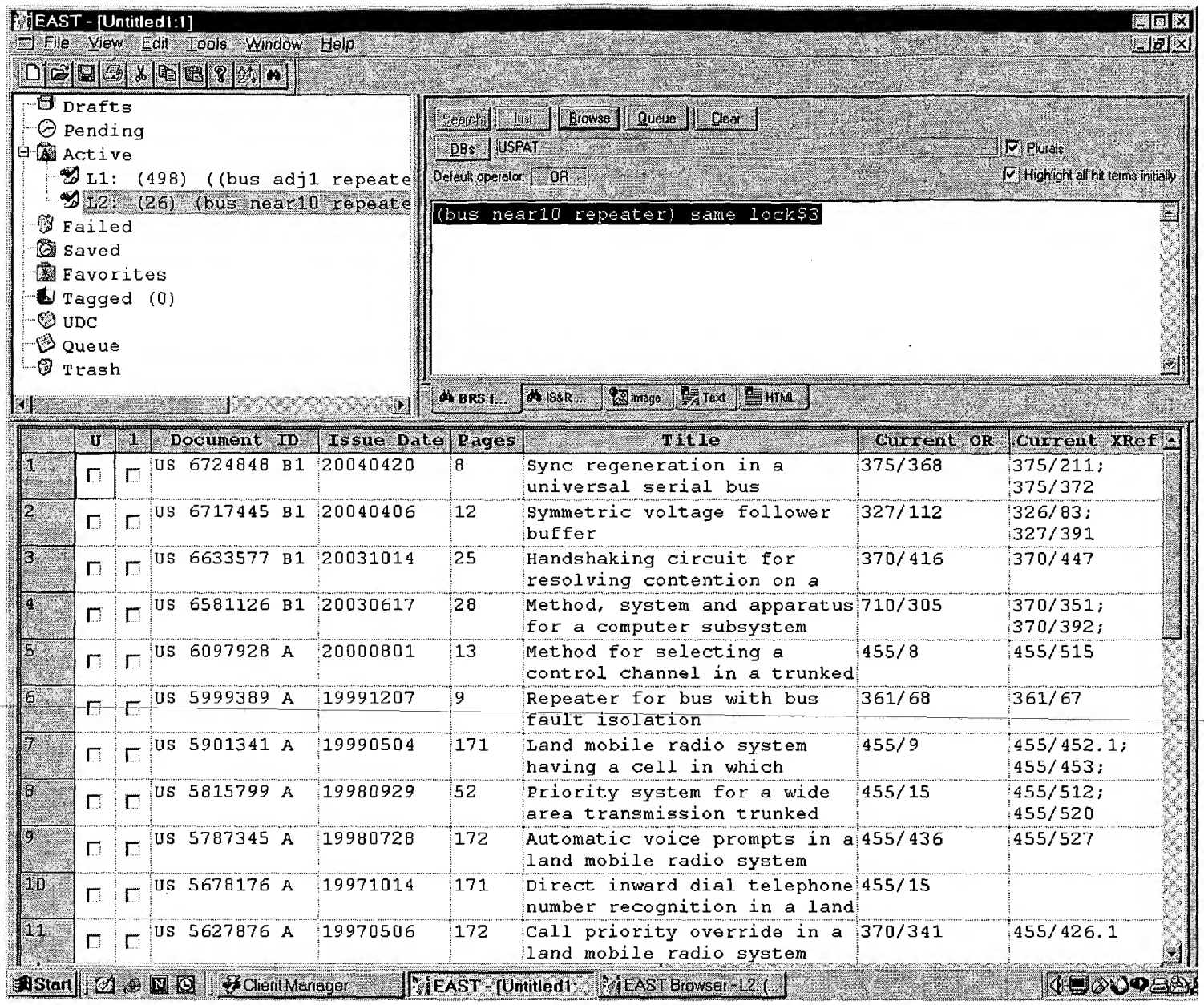
Set Name	Query
side by side	
	DB=USPT,USOC; PLUR=YES; OP=OR
L5	l2 and L4
L4	710/305,31,306,313,314,105,200;370/351,287,492,501;709/239,253;375/211;326/104;340/825.5.
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L3	L2
	DB=USPT,USOC; PLUR=YES; OP=OR
L2	((bus-repeater) or (bus adj1 repeater)) and lock$3
L1	((bus-repeater) or (bus adj1 repeater)) same lock$3

END OF SEARCH HISTORY

h e b b cg b e e ch



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	498	((bus adj1 repeater) or repeater) same lock$3	USPAT	2004/08/24 09:42			0
2	BRS	L2	26	(bus near10 repeater) same lock$3	USPAT	2004/08/24 09:43			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6724848 B1	20040420	8	Sync regeneration in a universal serial bus	375/368	375/211; 375/372
2	☐	☐	US 6717445 B1	20040406	12	Symmetric voltage follower buffer	327/112	326/83; 327/391
3	☐	☐	US 6633577 B1	20031014	25	Handshaking circuit for resolving contention on a	370/416	370/447
4	☐	☐	US 6581126 B1	20030617	28	Method, system and apparatus for a computer subsystem	710/305	370/351; 370/392;
5	☐	☐	US 6097928 A	20000801	13	Method for selecting a control channel in a trunked	455/8	455/515
6	☐	☐	US 5999389 A	19991207	9	Repeater for bus with bus fault isolation	361/68	361/67
7	☐	☐	US 5901341 A	19990504	171	Land mobile radio system having a cell in which	455/9	455/452.1; 455/453;
8	☐	☐	US 5815799 A	19980929	52	Priority system for a wide area transmission trunked	455/15	455/512; 455/520
9	☐	☐	US 5787345 A	19980728	172	Automatic voice prompts in a land mobile radio system	455/436	455/527
10	☐	☐	US 5678176 A	19971014	171	Direct inward dial telephone number recognition in a land	455/15	
11	☐	☐	US 5627876 A	19970506	172	Call priority override in a land mobile radio system	370/341	455/426.1

Your search matched **2** of **1064971** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

(bus repeater) or bus repeater<and>lock* Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **IEEE P1596, a scalable coherent interface for gigabyte/sec multiprocessor applications**
Gustavson, D.B.;
Nuclear Science, IEEE Transactions on , Volume: 36 , Issue: 1 , Feb. 1989
Pages:811 - 812

[Abstract] [PDF Full-Text (228 KB)] **IEEE JNL**

2 **Scalable coherent interface**
Gustavson, D.B.;
COMPCON Spring '89. Thirty-Fourth IEEE Computer Society International Conference: Intellectual Leverage, Digest of Papers. , 27 Feb.-3 March 1989
Pages:536 - 538

[Abstract] [PDF Full-Text (308 KB)] **IEEE CNF**

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Scalable coherent interface

Gustavson, D.B.
Stanford Linear Accel. Center, CA, USA ;

This paper appears in: **COMPCON Spring '89. Thirty-Fourth IEEE Comput International Conference: Intellectual Leverage, Digest of Papers.**

Meeting Date: 02/27/1989 - 03/03/1989
Publication Date: 27 Feb.-3 March 1989
Location: San Francisco, CA USA
On page(s): 536 - 538
Reference Cited: 0
Inspec Accession Number: 3406265

Abstract:
The scalable coherent interface (SCI) project (formerly known as SuperBus) i: experience gained during the development of Fastbus (IEEE 960), Futurebus (896.1) and other modern 32-bit buses. SCI goals include a minimum bandwic Gb/s per processor; efficient support of a coherent distributed-cache image of memory; and support for segmentation, **bus repeaters**, and general switche interconnections like Banyon, Omega, or full crossbars. SCI abandons the imr handshake characteristics of the present generation of buses in favor of a pac protocol. SCI avoids wire-ORs, broadcasts, and even ordinary passive bus stri except that a lower-performance (1 Gb/s per backplane instead of per proces implementation using a register insertion ring architecture on a passive backp appears to be possible using the same interface as for the more costly switch summary is presented of current directions, and the status of the work in pro reported

Index Terms:
computer interfaces 1 Gbit/s Banyon Omega SuperBus **bus repeaters** coherent cache image full crossbars general switched interconnections handshake characteris based protocol register insertion ring architecture scalable coherent interface segme shared memory

h eee e eee g e ch ch b c be be

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 8 of 8 returned.

☐ 1. Document ID: US 6724848 B1

Using default format because multiple data bases are involved.

L5: Entry 1 of 8 File: USPT Apr 20, 2004

US-PAT-NO: 6724848
DOCUMENT-IDENTIFIER: US 6724848 B1

TITLE: Sync regeneration in a universal serial bus

DATE-ISSUED: April 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Iyer; Venkat	Beaverton	OR		

US-CL-CURRENT: 375/368; 375/211, 375/372

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

☐ 2. Document ID: US 6636921 B1

L5: Entry 2 of 8 File: USPT Oct 21, 2003

US-PAT-NO: 6636921
DOCUMENT-IDENTIFIER: US 6636921 B1

TITLE: SCSI repeater circuit with SCSI address translation and enable

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWMC | Draw De

☐ 3. Document ID: US 6581126 B1

L5: Entry 3 of 8 File: USPT Jun 17, 2003

US-PAT-NO: 6581126
DOCUMENT-IDENTIFIER: US 6581126 B1

TITLE: Method, system and apparatus for a computer subsystem interconnection using a chain of bus repeaters

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 4. Document ID: US 6513085 B1

L5: Entry 4 of 8 File: USPT Jan 28, 2003

US-PAT-NO: 6513085
DOCUMENT-IDENTIFIER: US 6513085 B1

TITLE: Link/transaction layer controller with integral microcontroller emulation

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 5. Document ID: US 6493785 B1

L5: Entry 5 of 8 File: USPT Dec 10, 2002

US-PAT-NO: 6493785
DOCUMENT-IDENTIFIER: US 6493785 B1

TITLE: Communication mode between SCSI devices

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 6. Document ID: US 5684966 A

L5: Entry 6 of 8 File: USPT Nov 4, 1997

US-PAT-NO: 5684966
DOCUMENT-IDENTIFIER: US 5684966 A

TITLE: Method for operating a repeater for distributed arbitration digital data buses

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 7. Document ID: US 5613077 A

L5: Entry 7 of 8 File: USPT Mar 18, 1997

US-PAT-NO: 5613077
DOCUMENT-IDENTIFIER: US 5613077 A

TITLE: Method and circuit for communication between a module and a bus controller in a wafer-scale integrated circuit system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

h e b b g e e e f e bgc ef b e

☐ 8. Document ID: US 4974153 A

L5: Entry 8 of 8 File: USPT Nov 27, 1990

US-PAT-NO: 4974153
DOCUMENT-IDENTIFIER: US 4974153 A

TITLE: Repeater interlock scheme for transactions between two buses including transaction and interlock buffers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L2 and L4	8

Display Format: - Change Format

Previous Page Next Page Go to Doc#

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First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L5: Entry 3 of 8 File: USPT Jun 17, 2003

US-PAT-NO: 6581126
DOCUMENT-IDENTIFIER: US 6581126 B1

TITLE: Method, system and apparatus for a computer subsystem interconnection using a chain of bus repeaters

DATE-ISSUED: June 17, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Regula; Jack	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
PLX Technology, Inc.	Sunnyvale	CA			02

APPL-NO: 09/ 315412 [PALM]
DATE FILED: May 19, 1999

PARENT-CASE:
This application is a continuation-in-part of copending U.S. application Ser. No. 08/771,581, Method and Apparatus for a Fault Tolerant, Software Transparent and High Data Integrity Extension to a Backplane Bus or Interconnect filed Dec. 20, 1996 and hereby incorporated by reference in its entirety; this application also claims priority to U.S. Provisional application No. 60/116,686, Broken Ring, filed Jan. 20, 1999, and hereby incorporated by reference in its entirety.

INT-CL: [07] G06 F 13/28, G06 F 13/14, G06 F 15/173, H04 L 12/28, H04 L 12/56

US-CL-ISSUED: 710/305; 710/31, 370/351, 370/392, 709/239, 709/242
US-CL-CURRENT: 710/305; 370/351, 370/392, 709/239, 709/242, 710/31

FIELD-OF-SEARCH: 710/305, 710/31, 710/36-38, 370/223, 370/351, 370/392-393, 713/400-601, 709/238, 709/239, 709/240, 709/241, 709/242

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4727370	February 1988	Shih	340/3.9
☐	4736393	April 1988	Grimes et al.	

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☐	4845709	July 1989	Matsumoto et al.	
☐	4866706	September 1989	Christophersen et al.	370/85.7
☐	4882704	November 1989	Komori et al.	710/105
☐	4939752	July 1990	Literati et al.	
☐	4954983	September 1990	Klingman	710/11
☐	5155843	October 1992	Stamm et al.	714/5
☐	5241543	August 1993	Amada et al.	
☐	5410723	April 1995	Schmidt et al.	710/57
☐	5465251	November 1995	Judd et al.	370/54
☐	5734685	March 1998	Bedell et al.	375/356
☐	5764924	June 1998	Hong	
☐	5826037	October 1998	Stiegler et al.	395/200.81
☐	5828670	October 1998	Narasimha et al.	
☐	5841989	November 1998	James et al.	709/239
☐	5897656	April 1999	Vogt et al.	711/141
☐	5920267	July 1999	Tattersall et al.	340/825.05
☐	5964845	October 1999	Braun et al.	709/400

OTHER PUBLICATIONS

Efficient broadcast using selective flooding; Arunkumar, S.; Panwar, R.S.; Infocom '92. Eleventh Annual Joint Conference of the IEEE Computer and Communications Societies. IEEE, May 4-8, 1992 pp.: 2060-2067 vol. 3.*
A new flooding routing algorithm based on `node-step` concept ; Sheng-Lin; Jing-Sheng Liu; Singapore ICCS/ISITA '92. `Communications on the Move` , Nov. 16-20, 1992 pp.: 1396-1399 vol. 3.*
Towards a self-healing intelligent network; May, C.J.; Dighe, R.S.; Communications, 1991. ICC 91, Conference Record. IEEE International Conference on, Jun. 23-26, 1991 pp.: 655 -659 vol. 2.*
Master Thesis by Ivan Tving, Aug. 28, 1994, "Multiprocessor interconnection using SCI".
PCI Local Bus Specification, Revision 2.1, Jun. 1, 1995, PCI Special Interest Group.
PCT To PCI Bridge Architecture Specification, Version 1.0, 1994, PCI Special Interest Group.
Cache Coherence Protocols for Large-Scale Multiprocessors, by David Lars Chaiken.

ART-UNIT: 2189

PRIMARY-EXAMINER: Auve; Glenn A.

ASSISTANT-EXAMINER: Vu; Trisha

ATTY-AGENT-FIRM: Swernofsky Law Group PC

ABSTRACT:

The invention discloses methods and apparatus for broadcasting information across an interconnect that includes a plurality of nodes each connected to its adjacent

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node(s) using one or more links. The nodes can emit cells containing transaction sub-actions onto the links. As a node receives a cell the node retransmits the cell onto other links as the cell is being received. Thus, reducing the latency imposed by the node. The node also captures the transaction sub-action while it the cell is retransmitted. The node responds to the transaction sub-action by manipulating shared handshake lines that are bussed with the other nodes. The invention enables snooping cache protocols to be successfully used in a larger multi-processor computer system than the prior art.

69 Claims, 13 Drawing figures

Previous Doc Next Doc Go to Doc#

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US006581126B1

(12) **United States Patent**
Regula

(10) **Patent No.: US 6,581,126 B1**
(45) **Date of Patent: Jun. 17, 2003**

(54) **METHOD, SYSTEM AND APPARATUS FOR A COMPUTER SUBSYSTEM INTERCONNECTION USING A CHAIN OF BUS REPEATERS**

(75) Inventor: **Jack Regula**, San Jose, CA (US)

(73) Assignee: **PLX Technology, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/315,412**

(22) Filed: **May 19, 1999**

Related U.S. Application Data

(63) Continuation-in-part of application No. 08/771,581, filed on Dec. 20, 1996.

(60) Provisional application No. 60/116,586, filed on Jan. 20, 1999.

(51) **Int. Cl.**[7] **G06F 13/28**; G06F 13/14; G06F 15/173; H04L 12/28; H04L 12/56

(52) **U.S. Cl.** **710/305**; 710/31; 370/351; 370/392; 709/239; 709/242

(58) **Field of Search** 710/305, 31, 36–38; 370/223, 351, 392–393; 713/400–501; 709/238, 239, 240, 241, 242

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,727,370	A	*	2/1988	Shih 340/3.9
4,736,393	A		4/1988	Grimes et al.
4,845,709	A		7/1989	Matsumoto et al.
4,866,706	A		9/1989	Christopherson et al. .. 370/85.7
4,882,704	A	*	11/1989	Komori et al. 710/105
4,939,752	A		7/1990	Litsrail et al.
4,954,985	A	*	9/1990	Klingman 710/11
5,155,543	A	*	10/1992	Stamm et al. 714/5
5,241,543	A		8/1993	Amada et al.
5,410,723	A	*	4/1995	Schmidt et al. 710/57
5,465,251	A		11/1995	Judd et al. 370/54
5,734,685	A	*	3/1998	Bedell et al. 375/356
5,764,924	A		6/1998	Hong
5,828,037	A		10/1998	Stiegler et al. 395/200.81
5,828,670	A		10/1998	Narasimha et al.
5,841,989	A	*	11/1998	James et al. 709/239
5,897,656	A	*	4/1999	Vogt et al. 711/141
5,920,267	A		7/1999	Tatsenall et al. 340/825.05
5,964,845	A	*	10/1999	Braun et al. 709/400

OTHER PUBLICATIONS

Efficient broadcast using selective flooding; Arunkumar, S.; Panwar, R.S.; Infocom '92. Eleventh Annual Joint Conference of the IEEE Computer and Communications Societies. IEEE, May 4–8, 1992 pp.: 2060–2067 vol. 3.*

A new flooding routing algorithm based on 'node-step' concept ; Sheng-Lin; Jing-Sheng Liu; Singapore ICCS/ISITA '92. 'Communications on the Move' , Nov. 16–20, 1992 pp.: 1396–1399 vol. 3.*

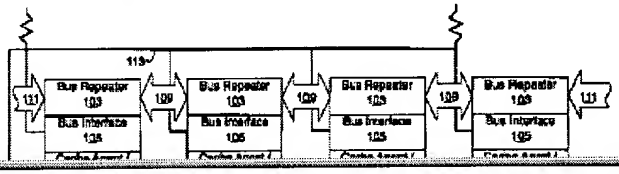
(List continued on next page.)

Primary Examiner—Glenn A. Auve
Assistant Examiner—Trisha Vu
(74) *Attorney, Agent, or Firm*—Swernofsky Law Group PC

(57) **ABSTRACT**

The invention discloses methods and apparatus for broadcasting information across an interconnect that includes a plurality of nodes each connected to its adjacent node(s) using one or more links. The nodes can emit cells containing transaction sub-actions onto the links. As a node receives a cell the node retransmits the cell onto other links as the cell is being received. Thus, reducing the latency imposed by the node. The node also captures the transaction sub-action while it the cell is retransmitted. The node responds to the transaction sub-action by manipulating shared handshake lines that are bussed with the other nodes. The invention enables snooping cache protocols to be successfully used in a larger multi-processor computer system than the prior art.

69 Claims, 12 Drawing Sheets



US005999389A

United States Patent [19]

Luebke et al.

[11] Patent Number: 5,999,389

[45] Date of Patent: Dec. 7, 1999

[54] **REPEATER FOR BUS WITH BUS FAULT ISOLATION**

[75] Inventors: Charles J. Luebke, Sussex; Walter L. Rutchik, New Berlin, both of Wis.

[73] Assignee: Eaton Corporation, Cleveland, Ohio

[21] Appl. No.: 08/736,120

[22] Filed: Oct. 24, 1996

[51] Int. Cl.[6] H02H 3/00

[52] U.S. Cl. 361/68; 361/67

[58] Field of Search 361/78–79, 81, 361/83, 62–68; 375/211, 214; 379/338–345, 348

[56] References Cited

U.S. PATENT DOCUMENTS

3,659,055 4/1972 Wilmore 375/214

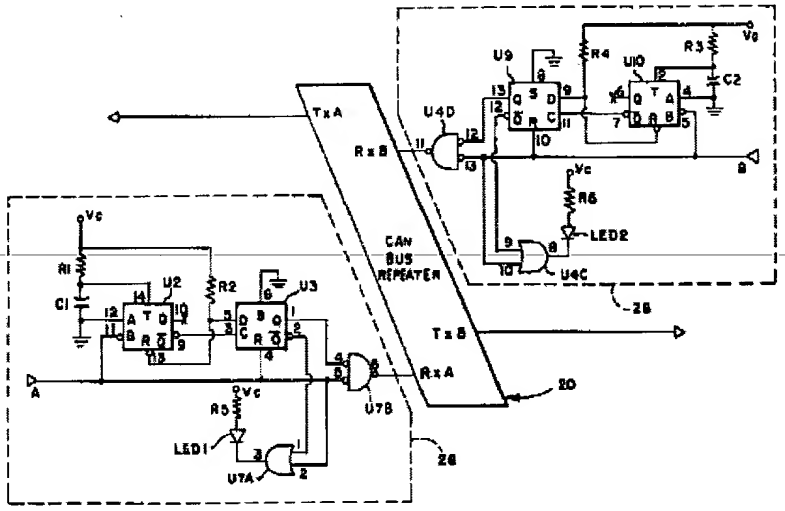
Primary Examiner—Michael J. Sherry

Attorney, Agent, or Firm—Charles E. Kosinski

[57] **ABSTRACT**

A repeater for a communication network having an isolation circuit for disabling the transmission of a fault-indicative signal through the repeater onto the network. A retriggerable one-shot starts timing with high to low signal transition. In the absence of a second transition within a defined time period, the one-shot triggers a flip-flop which, depending on the logic level of the input signal, generates an enabling signal passed to a logic gate to selectively allow and cut off the transmission of the signal to the repeater circuit input.

31 Claims, 4 Drawing Sheets



US005999389A

United States Patent [19]

Luebke et al.

[11] Patent Number: 5,999,389

[45] Date of Patent: Dec. 7, 1999

[54] **REPEATER FOR BUS WITH BUS FAULT ISOLATION**

[75] Inventors: Charles J. Luebke, Sussex; Walter L. Rutchik, New Berlin, both of Wis.

[73] Assignee: Eaton Corporation, Cleveland, Ohio

[21] Appl. No.: 08/736,120

[22] Filed: Oct. 24, 1996

[51] Int. Cl.[6] H02H 3/00

[52] U.S. Cl. 361/68; 361/67

[58] Field of Search 361/78–79, 61, 361/83, 62–68; 375/211, 214; 379/338–345, 348

[56] References Cited

U.S. PATENT DOCUMENTS

3,659,055 4/1972 Wilmore 375/214

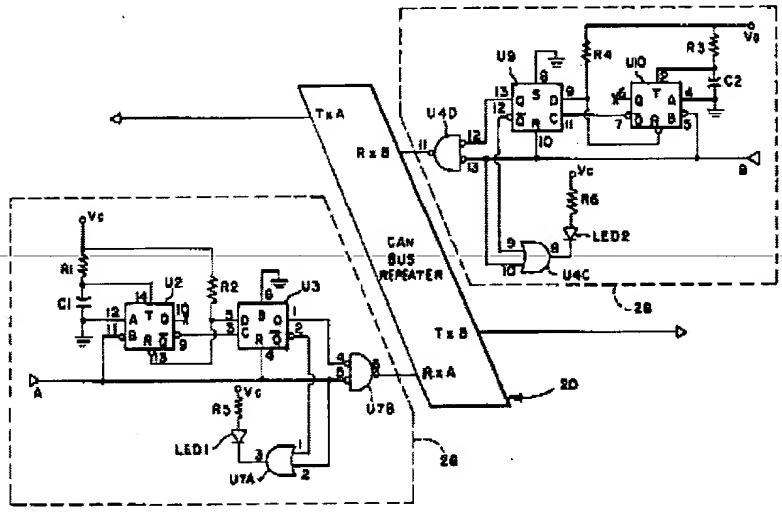
Primary Examiner—Michael J. Sherry

Attorney, Agent, or Firm—Charles E. Kosinski

[57] **ABSTRACT**

A repeater for a communication network having an isolation circuit for disabling the transmission of a fault-indicative signal through the repeater onto the network. A retriggerable one-shot starts timing with high to low signal transition. In the absence of a second transition within a defined time period, the one-shot triggers a flip-flop which, depending on the logic level of the input signal, generates an enabling signal passed to a logic gate to selectively allow and cut off the transmission of the signal to the repeater circuit input.

31 Claims, 4 Drawing Sheets



US005430726A

United States Patent [19]

Moorwood et al.

[11] Patent Number: 5,430,726

[45] Date of Patent: Jul. 4, 1995

[54] **REPEATER INTERFACE CONTROLLER WITH A SHARED DATA BUS**

[76] Inventors: Charles A. Moorwood, 1041 Lanark Ct., Sunnyvale, Calif. 94087; Charan J. Singh, 5077 Silverado Dr., Fairfield, Calif. 94533

[21] Appl. No.: 939,086

[22] Filed: Sep. 2, 1992

Related U.S. Application Data

[62] Division of Ser. No. 643,208, Jan. 18, 1991, abandoned.

[51] Int. Cl.[6] H04J 3/26; H04L 12/36

[52] U.S. Cl. 370/88.11; 370/94.1; 370/110.1

[58] Field of Search 370/17.60, 85.9, 85.11, 370/85.13, 94.1, 110.1, 85.6

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,232,386	11/1980	McDonald et al.	370/56
4,451,916	5/1984	Casper et al.	370/16
4,672,601	6/1987	Ablay	370/31
4,768,188	8/1988	Barnhart et al.	370/80
4,777,633	10/1988	Fletcher et al.	370/109
4,792,948	12/1988	Haugen	370/66
4,817,080	3/1989	Soha	370/17
4,825,435	4/1989	Amundsen et al.	370/97
4,945,533	7/1990	Hold	370/85.3

FOREIGN PATENT DOCUMENTS

0222669 5/1987 European Pat. Off. .

OTHER PUBLICATIONS

William Stallings, *Local Networks*, 3rd Edition, Macmillan Publishing Co., pp. 63–68; 90–99; and 155–165.

Willis Stallings, *Handbook of Computer Communications Standards* vol. 2, Howard W. Sams & Co., pp. 84–116.

ANSI/IEEE, *Supplements to LAN: CSMA/CD*, ANSI/IEEE, pp. 25–39.

Wescon Technical Papers, vol. 27, 1983, North Hollywood US pp. 1–4; G. Moseley: 'CMOS Manchester Code Converter for Local Area Networks'" p. 2, left column, line 31—p. 3, left column, line 6*.

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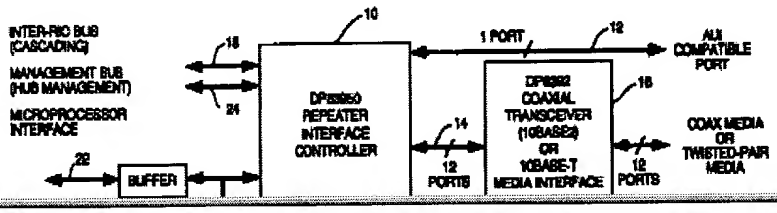
Attorney, Agent, or Firm—Limbach & Limbach

[57] **ABSTRACT**

A repeater interface controller receives a data packet at one of a plurality of port nodes from an associated segment of a local area network. The plurality of port nodes determine a priority port node when more than one port node receives a data packet at substantially the same time. The priority port node transmits the data packet from the priority port node to a central node. The central node receives the data packet from the priority node, repeats the data packet, and transmits the repeated data packet to the non-priority port nodes. Each non-priority port node receives the repeated data packet and transmits the repeated data onto its associated segment. Management and status information is transferred between the port nodes and an external processor and an external display by an internal bus and an external bus. A bus arbiter alternately provides a bus controller and the external controller control of both the internal and external buses to transfer the data. The bus controller controls both the internal and external buses when management and status data is transferred from the port nodes to the external display and the external controller controls both buses when management and status information is transferred between the external controller and the port nodes.

16 Claims, 59 Drawing Sheets



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United States Patent [19]

Shah

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[45] Date of Patent: Mar. 29, 1994

[54] **REPEATER INTERFACE CONTROLLER WITH MULTIPLE PORT NODE INTERFACES**

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[21] Appl. No.: 930,712

[22] Filed: Aug. 14, 1992

Related U.S. Application Data

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[51] Int. Cl.[5] H04J 3/26

[52] U.S. Cl. 370/85.6; 370/85.13; 370/94.3; 370/97

[58] Field of Search 370/60, 94.1, 94.3, 370/13.1, 85.6, 85.9, 85.11, 85.12, 85.13, 95.3, 97; 340/825.5, 825.02

[56] References Cited

U.S. PATENT DOCUMENTS

4,232,386	11/1980	McDonald et al.	370/56
4,451,916	5/1984	Casper et al.	370/16
4,672,601	6/1987	Abley	370/31
4,768,188	8/1988	Barnhart et al.	370/80
4,777,653	10/1988	Fletcher et al.	370/109
4,792,948	12/1988	Hangen	370/66
4,817,080	3/1989	Soha	370/17
4,825,435	4/1989	Amundsen et al.	370/97
4,908,530	3/1990	Huang	370/94.1
4,945,532	7/1990	Hold	370/85.3

FOREIGN PATENT DOCUMENTS

0222659 5/1987 European Pat. Off. .

OTHER PUBLICATIONS

William Stallings, *Local Networks*, 3rd Edition, Macmillan Publishing Co., pp. 63-68; 90-99; and 153-165.

William Stallings, *Handbook of Computer Communications Standards*, vol. 2, Howard W. Sams & Co., pp. 84-116.

ANSI/IEEE, *Supplements to LAN: CSMA/CD*, ANSI/IEEE, pp. 25-39, Std 802.3c-1985, Std 802.3d-1987.

Wescon Technical Papers, vol. 27, 1983, North Hollywood US pp. 1-4; G. Moesleyn 'CMOS Manchester Code Converter for Local Area Networks' * p. 2, left column, line 31-p. 3, left column, line 6*.

Primary Examiner—Douglas W. Olms
Assistant Examiner—Melvin Marcelo
Attorney, Agent, or Firm—Limbach & Limbach

[57] ABSTRACT

A repeater interface controller receives a data packet at one of a plurality of port nodes from an associated segment of a local area network. At least one port node is configurable as either an attachment unit interface or a twisted pair interface. The port nodes determine a priority port node, of more than one port node receives a data packet at substantially the same time, and transmit the data packet from the priority port node to a central node. The central node receives the data packet from the priority node, repeats the data packet, and transmits the repeated data packet to the non-priority port nodes. Each non-priority port node receives the repeated data packet and transmits the repeated data onto its associated segment.

14 Claims, 89 Drawing Sheets